Reliability Report

General Information	
Product Line	*MV3S*
Product Description	*powerSTEP*
Product division	*I&PC*
Package	*VFQFPN 11x14*
Silicon process technology	*BCD6S (UA53) + PMOS OFT1 (OD0C)*

Locations	
Wafer fab location	*CATANIA*
Assembly plant location	*CARSEM-S MALAYSIA*
Preliminary Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	02-Feb-16	14	G. D'Angelo	Original document
1.1	19-Oct-16	14	G. D'Angelo	Updated report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of MV3S device diffused in CATANIA and assembled in VFQFPN 11x14 in CARSEM-S MALAYSIA.
According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- High Temperature Storage Life

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed **the MV3S diffused in CATANIA and assembled in VFQFPN 11x14 in CARSEM-S MALAYSIA can be qualified from reliability viewpoint.**

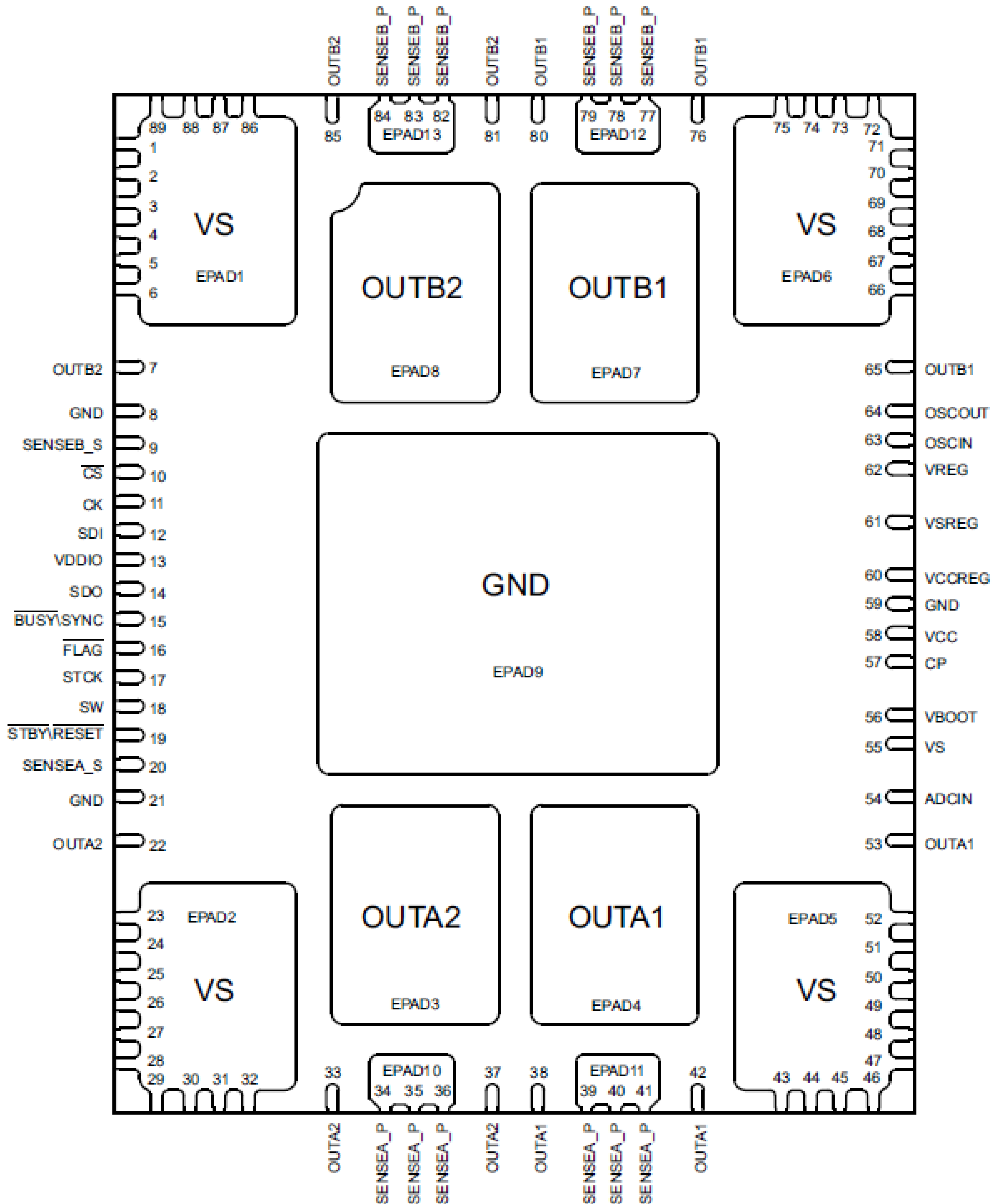
3 DEVICE CHARACTERISTICS

3.1 Device description

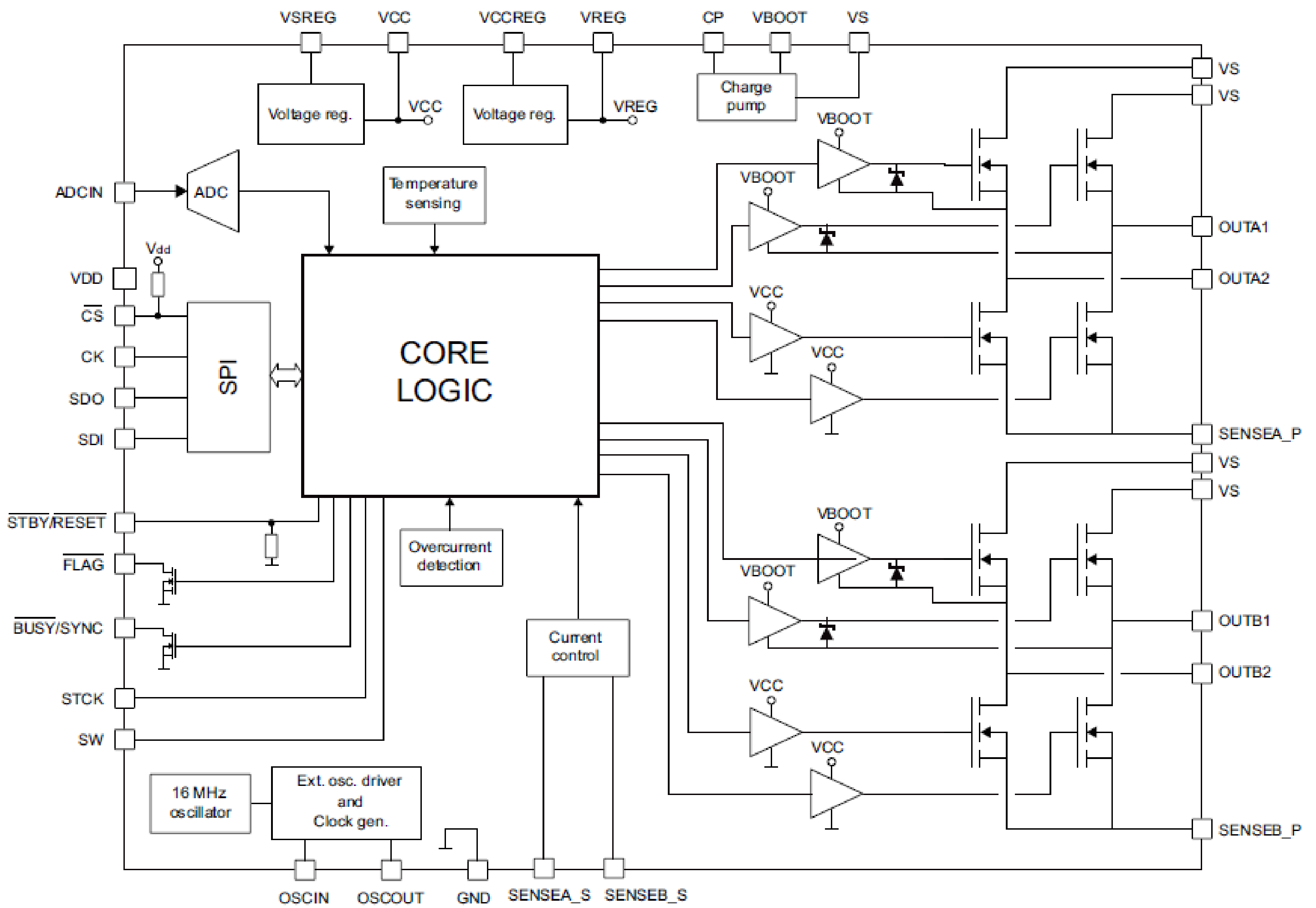
3.1.1 Generalities

The MV3S is a system-in-package integrating 8 N-channel 16 mΩ MOSFETs for stepper applications up to 85 V with a SPI programmable controller, providing fully digital control of the motion through a speed profile generation and positioning calculations.
It integrates a dual low $R_{DS\ (on)}$ full bridge with embedded non-dissipative overcurrent protection. The device can operate with both voltage mode driving and advanced current control fitting different application needs.

3.1.1 Pin connection

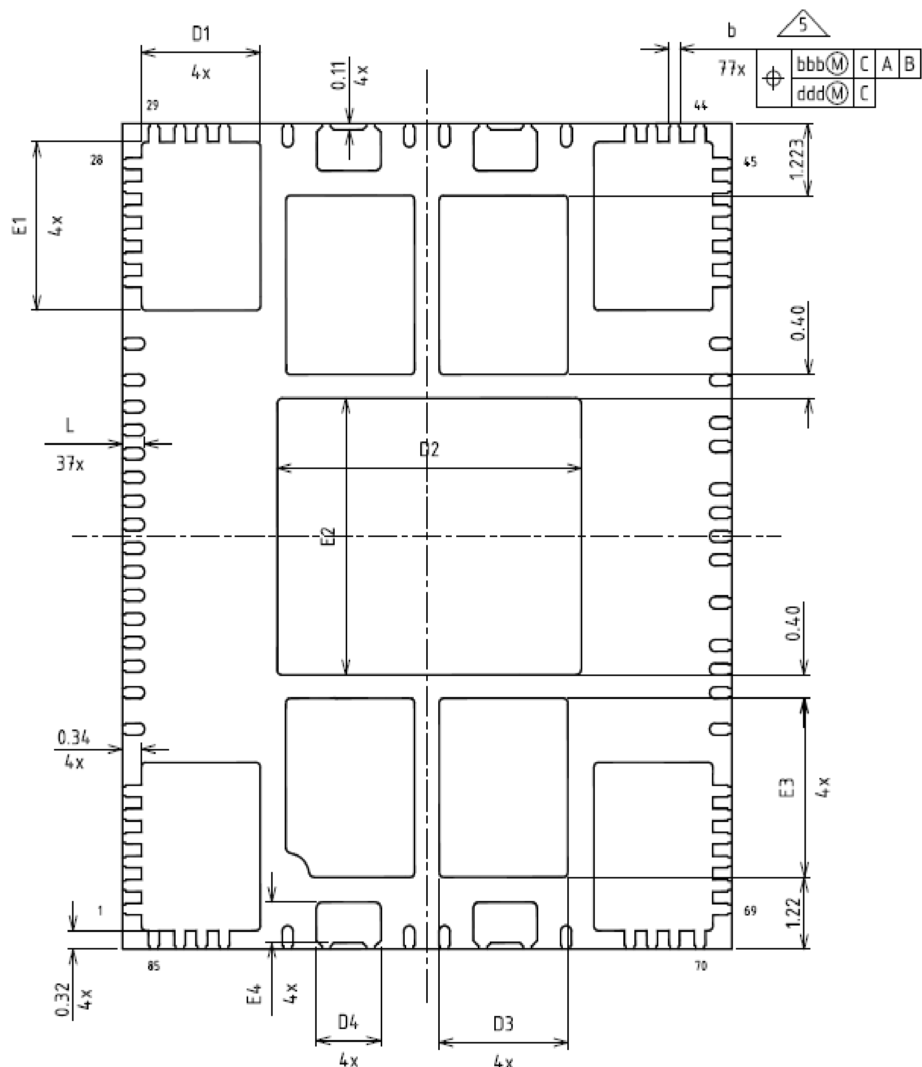


3.1.2 Block diagram



3.1.3 Package outline/Mechanical data

	DATABOOK (mm)		
REF.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.2	0.25
D	11 BSC		
E	14 BSC		
D1	2	2.15	2.25
E1	2.1	2.85	2.95
D2	5.35	5.5	5.6
E2	4.54	4.69	4.19
D3	2.11	2.32	2.42
E3	2.88	3.03	3.13
D4	1	1.15	1.25
E4	0.54	0.69	0.19
L	0.3	0.4	0.5
aaa	0.05		
bbb	0.1		
ccc	0.1		
ddd	0.05		
eee	0.08		
N	85		



3.2 Traceability

Wafer fab information (UA53)	
Wafer fab manufacturing location	*CATANIA*
Wafer diameter	*8 inches*
Wafer thickness	*280µm*
Silicon process technology	*BCD6S*
Die finishing back side	*Cr/NiV/Au*
Die size	*2185x3772 µm*
Bond pad metallization layers	*AlCu/TiNARC*
Passivation	*TEOS/SiN/Polymide*
Metal levels	*4*
Wafer fab information (OD0C)	
Wafer fab manufacturing location	*CATANIA*
Wafer diameter	*8 inches*
Wafer thickness	*200µm*
Silicon process technology	*P.MOSFET OFT1*
Die finishing back side	*Ti/NiV/Ag*
Die size	*1800x2500 µm*
Bond pad metallization layers	*AlCu/Ti/TiN*
Passivation	*TEOS/SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*CARSEM-S MALAYSIA*
Package description	*VFQFPN 11x14*
Molding compound	*G770 family*
Wires bonding materials/diameters	*Cu 2.0 mils / 1.3 mils*
Die attach material	*QMI529HT glue for PMOS die* *QMI519 (UA53 die)*
Lead solder material	*Sn*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Rev.	Comments
1a,1b,1c	AAA	No Passivation on MOS
2,3,4	AAA	-

4.2 Test plan and results summary

Die Oriented Tests							
Test	Method	Conditions	Sample Size			Duration	Results
			Lot 1a	Lot 1b	Lot 1c		
HTOL	High Temperature Operating Life						
	On chipboards	Tj=150°C Vs=85V	77	-	-	1000h	PASSED
HTSL	High Temperature Storage						
	No bias	Tamb=150°C	25	25	25	1000h	PASSED

Package Oriented Tests							
Test	Method	Conditions	Sample Size			Duration	Results
			Lot 2	Lot 3	Lot 4		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	75	75	75	-	PASSED
AC	Autoclave						
	PC before	121°C 2atm	25	25	25	96h	PASSED
TC	Temperature Cycling						
	PC before	Temp. range: -50/+150°C	25	25	25	1000cy	PASSED
THB	Temperature Humidity Bias						
	PC before	Ta=85°C/85%RH Vboot=100V, Vs=85V	25	25	25	1000h	PASSED

Electrical Characterization Tests					
Test	Method	Conditions	Sample Size	Duration	Results
			Lot 1a		
ESD	Electro Static Discharge				
	Human Body Model	+/- 2kV	3	-	PASSED
	Charge Device Model	+/- 500V (750V on corner pins)	3	-	PASSED
LU	Latch-Up				
	Over-voltage and Current Injection	Tamb=125°C Jedec78	6	-	PASSED

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.3 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

5.2.4 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : Additional final test's site for POWERSTEP01 in ST Calamba (Philippines) and implementation of the passivated PMOS.
PCI Reference : AMG/17/10082

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

POWERSTEP01	POWERSTEP01TR	

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